PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-PWR/13/8223
Dated 20 Nov 2013

4D4K Front-End Capacity Extension - Ang Mo Kio (Singapore)

Table 1. Change Implementation Schedule

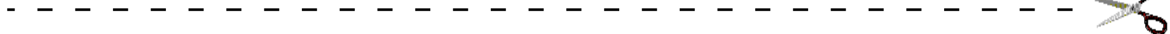
Forecasted implementation date for change	13-Nov-2013
Forecasted availability date of samples for customer	13-Nov-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	13-Nov-2013
Estimated date of changed product first shipment	15-May-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab process change
Reason for change	Improve service to Customers
Description of the change	Following the continuous improvement of our service and in order to rationalize and optimize Power MOSFET productivity, this document is announcing that the Production Line 4D4K, currently manufactured in Catania Wafer FAB, will be also produced in 6" wafer dimension in the ST's Ang Mo Kio (Singapore) plant. All commercials from 4D4K Line produced in Ang Mo Kio (Singapore), guarantee the same quality and electrical characteristics as reported in the relevant data sheet. Devices used for qualification are available as Samples.
Change Product Identification	by the digit 6 as front-end code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPD-PWR/13/8223**
Please sign and return to STMicroelectronics Sales Office	**Dated 20 Nov 2013**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Please be informed that the production Line 4D4K, currently manufactured in Catania Wafer FAB, will be also produced in 6” wafer dimension in the ST’s Ang Mo Kio (Singapore) plant.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 45-2013.

Product Family	Package	Part Number - Test Vehicle
Power MOSFET Transistor	PowerSO-10™	STV270N4F3

Change implementation schedule:

The first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power MOSFET Transistor	From Week 19-2014

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of Commercial Product produced from 4D4K Line, manufactured in in 6” wafer dimension in the ST’s Ang Mo Kio (Singapore) plant, will be ensured by the digit 6 as front-end code.

Sincerely Yours.

Reliability Report

4D4K Front-End Capacity Extension -
Ang Mo Kio (Singapore)

General Information	
Product Lines:	4D4K
Product Families:	Power MOSFET
P/Ns:	STV270N4F3
Product Group:	IMS - IPG
Product division:	Power Transistor Division
Package:	PowerSO-10™
Silicon Process techn.:	STripFET™ III

Locations	
Wafer Diffusion Plants:	*Ang Mo Kio (Singapore)*
EWS Plants:	*Ang Mo Kio (Singapore)*
Assembly plant:	*BOUSKOURA (Morocco)*
Reliability Lab:	*IMS-IPG Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	November 2013	8	C. Cappello	G. Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the Power MOSFET silicon line 4D4K made in Ang Mo Kio (Singapore) ST-Wafer Fab.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STV270N4F3 LINE: 4D4K PACKAGE: PowerSO-10™

Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	STripFET™ **III**
Die finishing back side	Ti/Ni/Au – Ti/Ni/Ag
Die size	6340 x 4600 μm^2
Metal	Al/Si/Cu
Passivation type	TEOS/NITRIDE

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Bouskoura (Morocco)
Package description	PowerSO-10™
Molding compound	Epoxy Resin
Frame material	Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Gate: Wire Al/Mg 5 mils Source: Ribbon Al 50x8 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Bouskoura (Morocco)
Tester	IP TEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STV270N4F3	4D4K	Power MOSFET
2	STV270N4F3	4D4K	Power MOSFET

5.2 Reliability test plan summary

Lot. 1&2 - D.U.T.: STV270N4F3 LINE: 4D4K PACKAGE: PowerSO-10™

#	Stress (Abrv)	PC	Std ref.	Conditions	Sample Size (S.S.)	Steps	Failure/SS		Family DATA (*)
							Lot 1	Lot 2	
1	TEST		User specification	All qualification parts tested per the requirements of the appropriate device specification.			0/462	0/462	
2	External visual		JESD22 B-101	All devices submitted for testing			0/462	0/462	
3	Parametric Verification		User specification	all parameters according to user specification from -55°C to 175°C	50		0/25	0/25	
4	Pre-conditioning		JESD22 A-113	Dryng 24H @ 125°C Store 168H @ TA=85°C RH=85% IR Reflow @ 245°C 3 times	All devices to be subjected to H3TRB, TC, AC, IOL		0/308	0/308	0/616
5	HTRB	N	JESD22 A-108	TA=175°C ; BIAS=32V TIME=1000 HOURS	154	168H	0/77	0/77	0/154
						500H	0/77	0/77	
						1000H	0/77	0/77	
6	HTGB	N	JESD22 A-108	TA=175°C ; BIAS=20V TIME=1000 HOURS	154	168H	0/77	0/77	0/154
						500H	0/77	0/77	
						1000H	0/77	0/77	
7	TC	Y	JESD22 A-104	TA=-55°C TO 150°C 1 HOURS / CYCLE TIME=1000CYCLES	154	100cy	0/77	0/77	0/154
						200cy	0/77	0/77	
						500cy	0/77	0/77	
						1000cy	0/77	0/77	
8	AC	Y	JESD22 A-102	TA=121°C ; PA=2ATM TIME=96H	154	96H	0/77	0/77	0/154
9	H3TRB	Y	JESD22 A-101	TA=85°C ; RH=85% BIAS=30V TIME=1000 HOURS	154	168H	0/77	0/77	0/154
						500H	0/77	0/77	
						1000H	0/77	0/77	
10	IOL / TF	Y	MIL-STD-750 Method 1037	ΔTC=105°C Ton / Toff = 3.5min	154	8.6Kcy	0/77	0/77	0/154

11	**ESD**		AEC Q101-001,002 and 005	CDM / HBM / MM	30		0/30		
12	**D.P.A.**		AEC-Q101-004 Section 4	Devices after H3TRB - TC	4		0/2	0/2	
13	**Thermal Resistance**		JESD24-3, 24-4, 24-6 as appropriate		10 pre & post change		0/10		
14	**Wire Bond Strength**		MIL-STD-750 Method 2037		10 bonds from min of 5 devices		0/50		
15	**Bond Shear**		AEC-Q101-003		10 bonds from min of 5 devices		0/50		
16	**Unclamped Inductive Switching**		AEC-Q101-004 Section 2		5		0/5		
17	**Dielectric Integrity**		AEC-Q101-004 Section 3		5		0/5		
18	**Die Shear**		MIL-STD-750 Method 2017		5		0/5		

(*) Family data: STripFET™ III Power MOSFET see following tables.

FAMILY DATA

Line: 4D5K Package..... H²PAK-6

Test	Test description	AEC Q101 S.S.	STM TEST CONDITIONS	STM S.S.	RESULTS Fail/s.s.
H.T.R.B.	High Temperature Reverse Bias	77 x 1 Lot	TA=175°C – BIAS=44V TIME=1000 HOURS	77	0/77
H.T.G.B.	High Temperature Foward Bias	77 x 1 Lot	TA=150°C – BIAS=20V TIME=1000 HOURS	77	0/77
PC	Preconditioning	All devices to be subjected to H3TRB, TC, AC,IOL	DRYNG 24H @ 125°C STORE 168H @ TA=85°C RH=85% Reflow @ 245°C 3 times	308	0/308
H3TRB	Temperature Humidity Reverse Bias	77 x 1 Lot	TA=85ºC – RH=85% - BIAS=50V TIME=1000 HOURS	77	0/77
AC	Autoclave	77 x 1 Lot	TA=121°C – PA=2ATM TIME=96h	77	0/77
TC	Temperature Cycling	77 x 1 Lot	-55°C TO 150°C 1 HOURS / CYCLE TIME=1000CYCLES	77	0/77
TF/IOL	Intermittent Operating Life	77 x 1 Lot	T on/off=3.5 min 8.6 Kcycles	77	0/77

Line: 4L63 Package..... PowerFLAT™ 5x6 D.I.

Test	Test description	AEC Q101 S.S.	STM TEST CONDITIONS	STM S.S.	RESULTS Fail/s.s.
H.T.R.B.	High Temperature Reverse Bias	77 x 1 Lot	TA=175°C – BIAS=48V TIME=1000 HOURS	77	0/77
H.T.G.B.	High Temperature Foward Bias	77 x 1 Lot	TA=150°C – BIAS=20V TIME=1000 HOURS	77	0/77
PC	Preconditioning	All devices to be subjected to H3TRB, TC, AC,IOL	DRYNG 24H @ 125°C STORE 168H @ TA=85°C RH=85% Reflow @ 260°C 3 times	308	0/308
H3TRB	Temperature Humidity Reverse Bias	77 x 1 Lot	TA=85ºC – RH=85% - BIAS=50V TIME=1000 HOURS	77	0/77
AC	Autoclave	77 x 1 Lot	TA=121°C – PA=2ATM TIME=96h	77	0/77
TC	Temperature Cycling	77 x 1 Lot	-55°C TO 150°C 1 HOURS / CYCLE TIME=1000CYCLES	77	0/77
TF/IOL	Intermittent Operating Life	77 x 1 Lot	T on/off=2 min 15 Kcycles	77	0/77

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

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